Sysnthesis utilization report

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| Tool Version : Vivado v.2021.1 (win64) Build 3247384 Thu Jun 10 19:36:33 MDT 2021

| Date : Wed Apr 10 16:09:28 2024

| Host : DESKTOP-4LK3EFH running 64-bit major release (build 9200)

| Command : report\_utilization -file UART\_utilization\_synth.rpt -pb UART\_utilization\_synth.pb

| Design : UART

| Device : 7z020clg400-1

| Design State : Synthesized

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Utilization Design Information

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1. Slice Logic

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| Slice LUTs\* | 6825 | 0 | 0 | 53200 | 12.83 |

| LUT as Logic | 6825 | 0 | 0 | 53200 | 12.83 |

| LUT as Memory | 0 | 0 | 0 | 17400 | 0.00 |

| Slice Registers | 16716 | 0 | 0 | 106400 | 15.71 |

| Register as Flip Flop | 16716 | 0 | 0 | 106400 | 15.71 |

| Register as Latch | 0 | 0 | 0 | 106400 | 0.00 |

| F7 Muxes | 2176 | 0 | 0 | 26600 | 8.18 |

| F8 Muxes | 1088 | 0 | 0 | 13300 | 8.18 |

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\* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt\_design after synthesis, if not already completed, for a more realistic count.

1.1 Summary of Registers by Type

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| Total | Clock Enable | Synchronous | Asynchronous |

+-------+--------------+-------------+--------------+

| 0 | \_ | - | - |

| 0 | \_ | - | Set |

| 0 | \_ | - | Reset |

| 0 | \_ | Set | - |

| 0 | \_ | Reset | - |

| 0 | Yes | - | - |

| 0 | Yes | - | Set |

| 171 | Yes | - | Reset |

| 0 | Yes | Set | - |

| 16545 | Yes | Reset | - |

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2. Memory

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+----------------+------+-------+------------+-----------+-------+

| Site Type | Used | Fixed | Prohibited | Available | Util% |

+----------------+------+-------+------------+-----------+-------+

| Block RAM Tile | 0 | 0 | 0 | 140 | 0.00 |

| RAMB36/FIFO\* | 0 | 0 | 0 | 140 | 0.00 |

| RAMB18 | 0 | 0 | 0 | 280 | 0.00 |

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\* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| DSPs | 0 | 0 | 0 | 220 | 0.00 |

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4. IO and GT Specific

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| Bonded IOB | 20 | 0 | 0 | 125 | 16.00 |

| Bonded IPADs | 0 | 0 | 0 | 2 | 0.00 |

| Bonded IOPADs | 0 | 0 | 0 | 130 | 0.00 |

| PHY\_CONTROL | 0 | 0 | 0 | 4 | 0.00 |

| PHASER\_REF | 0 | 0 | 0 | 4 | 0.00 |

| OUT\_FIFO | 0 | 0 | 0 | 16 | 0.00 |

| IN\_FIFO | 0 | 0 | 0 | 16 | 0.00 |

| IDELAYCTRL | 0 | 0 | 0 | 4 | 0.00 |

| IBUFDS | 0 | 0 | 0 | 121 | 0.00 |

| PHASER\_OUT/PHASER\_OUT\_PHY | 0 | 0 | 0 | 16 | 0.00 |

| PHASER\_IN/PHASER\_IN\_PHY | 0 | 0 | 0 | 16 | 0.00 |

| IDELAYE2/IDELAYE2\_FINEDELAY | 0 | 0 | 0 | 200 | 0.00 |

| ILOGIC | 0 | 0 | 0 | 125 | 0.00 |

| OLOGIC | 0 | 0 | 0 | 125 | 0.00 |

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5. Clocking

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| BUFGCTRL | 1 | 0 | 0 | 32 | 3.13 |

| BUFIO | 0 | 0 | 0 | 16 | 0.00 |

| MMCME2\_ADV | 0 | 0 | 0 | 4 | 0.00 |

| PLLE2\_ADV | 0 | 0 | 0 | 4 | 0.00 |

| BUFMRCE | 0 | 0 | 0 | 8 | 0.00 |

| BUFHCE | 0 | 0 | 0 | 72 | 0.00 |

| BUFR | 0 | 0 | 0 | 16 | 0.00 |

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6. Specific Feature

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| Site Type | Used | Fixed | Prohibited | Available | Util% |

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| BSCANE2 | 0 | 0 | 0 | 4 | 0.00 |

| CAPTUREE2 | 0 | 0 | 0 | 1 | 0.00 |

| DNA\_PORT | 0 | 0 | 0 | 1 | 0.00 |

| EFUSE\_USR | 0 | 0 | 0 | 1 | 0.00 |

| FRAME\_ECCE2 | 0 | 0 | 0 | 1 | 0.00 |

| ICAPE2 | 0 | 0 | 0 | 2 | 0.00 |

| STARTUPE2 | 0 | 0 | 0 | 1 | 0.00 |

| XADC | 0 | 0 | 0 | 1 | 0.00 |

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7. Primitives

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| Ref Name | Used | Functional Category |

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| FDRE | 16545 | Flop & Latch |

| LUT6 | 4818 | LUT |

| MUXF7 | 2176 | MuxFx |

| LUT5 | 1832 | LUT |

| MUXF8 | 1088 | MuxFx |

| FDCE | 171 | Flop & Latch |

| LUT3 | 90 | LUT |

| LUT2 | 71 | LUT |

| LUT4 | 39 | LUT |

| LUT1 | 34 | LUT |

| IBUF | 12 | IO |

| OBUF | 8 | IO |

| CARRY4 | 4 | CarryLogic |

| BUFG | 1 | Clock |

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8. Black Boxes

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| Ref Name | Used |

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9. Instantiated Netlists

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| Ref Name | Used |

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